**Studytonight – CAO test 4 – Aditya Jain**

1. **\_\_\_\_\_\_ serves as an intermediary between the device and the BUSes.**

**a) Interface circuits**b) Device drivers  
c) Buffers  
d) None of the mentioned

Explanation: The interface circuits act as a hardware interface between the device and the software side.

1. **The side of the interface circuits, that has the data path and the control signals to transfer data between interface and device is \_\_\_\_\_**

a) BUS side  
**b) Port side**c) Hardware side  
d) Software side

Explanation: This side connects the device to the motherboard.

1. **The interface circuits**

a) Helps in installing of the software driver for the device  
b) Houses the buffer that helps in data transfer  
**c) Helps in decoding of the address on the address BUS**  
d) None of the mentioned

Explanation: Once the address is put on the BUS, the interface circuit decodes the address and uses the buffer space to transfer data.

1. **The conversion from parallel to serial data transmission and vice versa takes place inside the interface circuits.  
   a) True**b) False

Explanation: By doing this, the interface circuits provides a better interconnection between devices.

1. **The DMA differs from the interrupt mode by**

a) The involvement of the processor for the operation  
b) The method accessing the I/O devices  
c) The amount of data transfer possible  
**d) None of the mentioned**

Explanation: DMA is an **approach** of performing data transfers in bulk between memory and the external device **without the intervention of the processor.**

1. **The DMA transfer is initiated by \_\_\_\_\_**

a) Processor  
**b) The program currently being executed**  
c) I/O devices  
d) OS

Explanation: The transfer can only be initiated by instruction of a program being executed.

1. **The registers of the controller are \_\_\_\_\_\_**

a) 64 bits  
b) 24 bits  
**c) 32 bits**d) 16 bits

1. **When process requests for a DMA transfer**

a) Then the process is temporarily suspended  
b) The process continues execution  
c) Another process gets executed  
**d) process is temporarily suspended & Another process gets executed**

Explanation: The process requesting the transfer is paused and the operation is performed, meanwhile another process is run on the processor.

1. **The technique where the controller is given complete access to main memory is**

a) Cycle stealing  
b) Memory stealing  
c) Memory Con  
**d) Burst mode**

Explanation: In **Burst Mode**, the controller is given full control of the memory access cycles and can **transfer blocks at a faster rate**.

1. **The controller uses \_\_\_\_\_ to help with the transfers when handling network interfaces.**

**a) Input Buffer storage**b) Signal enhancers  
c) Bridge circuits  
d) All of the mentioned

Explanation: The controller stores the data to be transferred in the buffer and then transfers it.

1. **To overcome the conflict over the possession of the BUS we use \_\_\_\_\_\_**

a) Optimizers  
**b) BUS arbitrators**  
c) Multiple BUS structure  
d) None of the mentioned

1. **The DMA transfers are performed by a control circuit called as**

a) Device interface  
**b) DMA controller**  
c) Data controller  
d) Overlooker

Explanation: The Controller performs the functions that would normally be carried out by the processor.

1. **After the completion of the DMA transfer the processor is notified by**

a) Acknowledge signal  
**b) Interrupt signal**c) WMFC signal  
d) None of the mentioned

Explanation: The controller raises an interrupt signal to notify the processor that the transfer was complete.

1. **When the R/W bit of the status register of the DMA controller is set to 1.**

a) **Read operation is performed**b) Write operation is performed  
c) Read & Write operation is performed  
d) None of the mentioned

1. **The DMA controller has \_\_\_\_\_\_\_ registers**

a) 4  
b) 2  
**c) 3**  
d) 1

Explanation: The Controller uses these three registers to store the **starting address, word count and the status of the operation.**